Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) The device of claim 13, further comprising:

a high voltage well of a first circuit device defined in the substrate; and

a first low voltage well of a second circuit device defined in the substrate.

2. (Canceled)

3. (Previously Presented) The device of claim 1, further comprising at least one microelectromechanical system-based element defined in the substrate.

4. (Original) The device of claim 1, wherein the substrate comprises a layer of silicon.

5. (Original) The device of claim 4, wherein the layer of silicon comprises p-type silicon.

6. (Original) The device of claim 1, wherein the substrate comprises a silicon-on-insulator wafer comprising a single-crystal-silicon layer, a substrate and an insulator layer therebetween.

7. (Original) The device of claim 6, wherein the single-crystal-silicon layer comprises p-type silicon.

8. (Original) The device of claim 1, further comprising a second low voltage well of the second circuit device defined in the substrate.

9. (Original) The device of claim 8, further comprising a field oxide layer over at least part of each of the high voltage well, the first low voltage well and the second low voltage well.

10. (Original) The device of claim 9, further comprising a polysilicon gate associated with each of the high voltage well, the first low voltage well and the second low voltage well.

11. (Original) The device of claim 10, further comprising:

a P-body defined in the high voltage well of the first circuit device;

an N+ source/drain defined in each of the P-body, the high voltage well and the first low voltage well of the second circuit device; and

a P+ source/drain in each of the P-body and the second low voltage well of the second circuit device.

12. (Original) The device of claim 11, further comprising:

a passivation oxide layer over at least the field oxide layer and the polysilicon gates;

a plurality of vias through the passivation oxide layer; and

a plurality of contacts, each of the contacts extending through the vias and contacting at least one of the sources/drains.

13. (Previously Presented) A heterogeneous device, comprising:

a substrate;

a plurality of heterogeneous circuit devices defined in the same substrate; and

a photodiode defined in the same substrate.

14. (Previously Presented) The device of claim 13, wherein the plurality of heterogeneous circuit devices comprises at lest one complementary metal oxide semiconductor transistor and at least one double-diffused metal oxide semiconductor transistor.

15-16. (Canceled)

17. (Original) The device of claim 13, wherein the substrate comprises a layer of silicon.

18. (Original) The device of claim 17, wherein the layer of silicon comprises p-type silicon.

19. (Original) The device of claim 13, wherein the substrate comprises a silicon-on-insulator wafer comprising a single-crystal-silicon layer, a substrate and an insulator layer therebetween.

20. (Original) The device of claim 19, wherein the single-crystal-silicon layer comprises p-type silicon.

21. (Previously Presented) A heterogeneous device, comprising:

a substrate;

a plurality of heterogeneous devices defined in the same substrate; and

at least one microelectromechanical system-based element defined in the same substrate.

22. (New) A heterogeneous device, comprising:

a substrate;

a plurality of heterogeneous circuit devices defined in the same substrate; and

at least one of a photodiode and a microelectromechanical system-based element defined in the same substrate.